REMARKS

The Drawings were objected to for containing a reference number (ref 32) which was not mentioned in the specification. Applicants have amended the specification as indicated herein to include reference number 32 in the description of the Figure 3. No amendments to the claims are presented at this time.

The Drawings were further objected to for failure to show every feature of the invention as recited in claims 2-14 and 16-42. Applicants respectfully traverse.

First, Applicants object to the Examiner's failure to specifically identify which limitations are allegedly not shown in the drawings.

Second, Applicants assert that the Drawings, taken in conjunction with the accompanying description, fully support the recited claims. Applicants have attached hereto, as Exhibit A, a listing of the claims 2-14 and 16-42 at issue as originally filed to which have been added notations, shown in **[bracketed bold characters]**, showing where the claimed feature may find support illustrated in the Drawings. In view of Exhibit A, Applicants respectfully request that the objection to the Drawings under 37 C.F.R 1.83(a) be withdrawn.

Applicants note for the record that the provided notations do not necessarily indicate the only Drawing support for the claimed limitations. Other portions of the Drawings may also support the claim limitations, especially when taken in the context of the accompanying description, and the notations are provided solely to show examples of where support may be found in the Drawings. At the Examiner's request, and with specific identification of the

limitations in question, Applicants can further provide cross-reference to specification support and other Drawing support for the recited claim limitations.

In view of the foregoing, Applicants respectfully request withdrawal of the objection to the Drawings.

Claims 2-14 and 16-42 were rejected under 35 U.S.C. 112, first paragraph, as not being enabled. Applicants respectfully traverse. As shown above, and in connection with the attached Exhibit A, Applicants have shown examples of how the claimed features are illustrated in the Drawings. Withdrawal of the rejection is requested.

Claims 1-29 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yoo. Applicants respectfully traverse.

Turning first to claim 1, Applicants claim "continuously and dynamically measuring the retention time of all the memory cells of the memory." In Yoo, a teaching is made for measuring data retention time of a DRAM (col. 3, lines 34-35), and then adjusting the self-refresh time period based on the measured data retention time (col. 3, lines 35-43). It is noted, however, that Yoo specifically teaches that the "self-refresh period is made (i.e., set) using a laser fuse in a wafer state or an electrical fuse once in a package state" (col. 3, lines 43-45). Thus, the self-refresh period is fixed by the utilized fuse structure and based on the data retention time measurement.

Applicants, on the other hand, specifically claim that retention time is continuously and dynamically measured with the refresh period set by those measurements. There is no teaching or suggestion in Yoo for the claimed continuous and dynamic measurement operation, or the use of such to effectuate a corresponding continuous and dynamic setting of the refresh period.

An advantage of Applicant's operation to continuously and dynamically measure retention time is that the refresh period can change and thus account for changes in temperature (see, specification Paragraphs [5], [25], [29], [31], [67], and [84]). Such cannot be achieved with Yoo's process and method where the refresh period is statically set by a fuse in response to a single data retention time measurement.

Claim 15 recites "a memory refreshing circuit that operates to continuously and dynamically measure the retention time of all the memory cells of the memory, and to regulate the refresh period of the memory based on the result of this measurement." Applicants respectfully submit that claim 15 distinguishes over Yoo for at least the same reasons as claim 1.

Withdrawal of the Section 103 rejection and allowance of claims 1-29 is accordingly requested.

Claims 30-42 were rejected under 35 U.S.C. 103(a) as being unpatentable over Frankowsky.

In claim 30, Applicants recite "in the meantime, continuing to refresh the non-selected memory cells within the memory at the current refresh rate." This "in the meantime" refreshing operation with respect to other cells occurs WHILE the retention rate of a selected group of cells is being tested (see, first two limitations of claim 30 and the common understanding of the phase "in the meantime"). This claimed process is quite distinct from the process disclosed by Frankowsky.

In Frankowsky, a refresh analysis circuit 20 operates to write test data into a portion of a memory and test data retention time for that portion. Once that portion has been examined, the circuit 20 moves on to test a next portion. This process repeats until all portions have been

tested. What is important to note with respect to the operation of the Frankowsky circuit 20 is that it is operable during memory set up and is used to set refresh rates for the various portions of the memory prior to its operational use. There is no "in the meantime" refreshing operation, with respect to the non-selected portions of the memory, taught by the process of Frankowsky. Instead, the retention time tests are performed by Frankowsky for each portion, and then at the end of the testing the determined minimum retention times are stored (col. 4, line 52) and a table of those times is later used to control when refresh occurs so as to save power in connection with operational use of the memory (col. 4, line 58).

In particular, Frankowsky teaches programming refresh addresses in response to determined retention times on an individual basis for each DRAM being manufactured (col. 5, lines 12-14). Subsequent operation of the memory for refresh operations is controlled by that programming (col. 5, lines 15-44). However, Frankowsky does not teach, during that subsequent normal operation, that the refresh rate analysis circuit 20 is in any way operational. Thus, there can be no "in the meantime" refreshing operation as is specifically claimed. This limitation emphasizes the "dynamically adjusting the refresh rate of a dynamic random access memory array" recitation provided in the preamble of claim 30. Frankowsky fails to teach or suggest any process for dynamically adjusting the refresh rate of a dynamic random access memory array where non-selected memory cells within the memory are refreshed at a current refresh rate while (i.e., in the meantime) test data content retention time is being measured with respect to selected memory cells.

An advantage of Applicant's "in the meantime" refreshing operation is that measurement of retention rate can be performed during operation of the memory and thus the refresh period

can change over time so as to account for changes in temperature (see, specification Paragraphs [5], [25], [29], [31], [67], and [84]). Such cannot be achieved with Frankowsky's process and method where the refresh period is statically set by the refresh circuit 20 (for example, at manufacture).

Claim 38 similarly recites "in the meantime, continuing to refresh the non-selected memory cells in accordance with their refresh rate." Applicants respectfully submit that claim 38 distinguishes over Fankowsky for at least the same reasons as claim 30.

Withdrawal of the Section 103 rejection and allowance of claims 30-42 is accordingly requested.

In view of the foregoing, Applicants respectfully submit that the application is in condition for favorable action and allowance.

Respectfully submitted,

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EXHIBIT A -

2. The process according to Claim 1, wherein continuously and dynamically measuring the retention time of all the memory cells comprises:

successively selecting different groups of cells of the memory in such a way as to scan the entire set of cells of the memory; **[states 30 and 41]**

successively measuring the retention times of each group of cells; **[states 33-35 and 37-39]** and

successively refreshing the unselected cells; **[state 36]**

wherein successively measuring comprises performing measurements on a selected group of cells at a lower measurement frequency than a refresh frequency of the unselected cells of the memory such that each selected group of cells is refreshed more slowly than unselected cells of the memory. **[states 33-35 and 37-39]**

3. The process according to Claim 2, wherein the memory is organized by pages, and each selected group of cells comprises an integer number of pages. **[see paragraph 54, CL RW]**

4. The process according to Claim 2,

wherein selectively measuring comprises:

writing predetermined test content to the selected group of cells; **[state 33]**

reading of the selected group of cells; **[state 38]** and

metering of a number of content errors in the reading of the selected group of cells in comparison to the predetermined test content; **[state 39]**

wherein selectively measuring the retention time comprises measuring the retention time of all the memory cells by an at least partial accumulation of the metered number of content errors; **[state 39]** and

wherein successively refreshing comprises refreshing the unselected cells of the memory at least twice in between the writing of the test content to the selected group of cells and the reading of the selected group of cells. **[states 36 and 37]**

5. The process according to Claim 4, wherein successively measuring further comprises, for at least one selected group of cells, backing up **[state 42]** of the content of the selected group of cells, and restoring **[state 40]** of the content of the selected group of cells with the backed up content following metering of the number of content errors.

6. The process according to Claim 4,

wherein successive measuring comprises writing of the test content into a first buffer memory before writing to the selected group of cells; **[state 32]** and

wherein reading of the test content from the selected group of cells comprises writing of the read content of the selected group of cells into a second buffer memory followed by reading of the second buffer memory. **[state 38]**

7. The process according to Claim 5, wherein backing up comprises storing in a predetermined part of the memory or else in an external backup memory. **[state 42, PM, CH0 AND CH1]**

8. The process according to Claim 6, wherein each selected group of cells forms a single page of the memory, and backing up comprises storing in one of the first and second buffer memories. **[paragraph 54, state 42, CH0 AND CH1]**

9. The process according to Claim 4, wherein regulating of the refresh period of the memory comprises:

comparing the metered number of accumulated errors with a low threshold and a high threshold; **[<, >, CMP2, SH1, SB1]**

increasing the refresh period if the metered number of accumulated errors is less than the low threshold; **[MUX2, CH, +]**

decreasing the refresh period if the metered number of accumulated errors is greater than the high threshold; **[MUX2, CB, -]** and

non-modifying the refresh period if the metered number of accumulated errors is greater than or equal to the low threshold and less than or equal to the high threshold. **[MUX2]**

10. The process according to Claim 4, wherein regulating of the refresh period of the memory comprises:

comparing the metered number of accumulated errors with a threshold; **[CMP2]**

increasing the refresh period if the metered number of errors is less than the threshold; **[CH, +, MUX2]** and

decreasing the refresh period if the metered number of errors is greater than or equal to the threshold. **[CB, -, MUX2]**

11. The process according to Claim 10, wherein refresh period has a minimum limit value and a maximum limit value. **[SH2, SB2]**

12. The process according to Claim 1, wherein continuously and dynamically measuring the retention time comprises performing retention time measurements for the cells of the memory cyclically, and tagging the cells of the memory having a lower retention time as measured in the course of a measurement cycle, **[step 45]** and wherein regulating the refresh period of the memory comprises setting the refresh period in the course of a next measurement cycle of the tagged cells to be refreshed more often than non-tagged cells of the memory. **[step 46]**

13. The process according to Claim 1, wherein the memory is incorporated into an apparatus **[TP]** which operates in both a standby mode and an active mode of operation, and wherein measuring and regulating are performed at least in the course of the standby mode.

14. The process according to Claim 13, wherein the apparatus is a handset **[TP]** of a wireless communication system.

16. The device according to Claim 15, wherein the memory refresh circuit comprises:

a selection circuit operating to perform successive selections of different groups of cells of the memory in such a way as to scan the entire set of cells of the memory; **[FSM, DCDL, states 30 and 41]**

a measurement circuit operating to perform successive measurements of the retention times of each selected group of cells; **[MAT, states 33-35 and 37-39]** and

a refresh circuit operating to perform successively refresh the unselected cells; **[CTLN, RF, state 36]**

wherein the measurement circuit is activated to perform measurements on a selected group of cells at a lower measurement frequency than a refresh frequency of the unselected cells of the memory such that selected groups of cells are refreshed more slowly than unselected cells of the memory. **[see, Q and q, and states 33-39]**

17. The device according to Claim 16, wherein the memory is organized by pages, and each selected group of cells comprises an integer number of pages. **[see paragraph 54, CL RW]**

18. The device according to Claim 16, wherein the measurement circuit comprises:

a storage device to store predetermined test content; **[RGT]**

a write circuit to write the predetermined test content to the selected group of cells; **[MUX1]**

a read circuit to read the selected group of cells; **[DO]**

a metering circuit to meter the number of content errors in the reading of the selected group of cells in comparison to the predetermined test content; **[LGC]** and

an accumulation circuit to perform an at least partial accumulation of the metered number of content errors; **[+, RG2]** and

wherein the refresh circuit refreshes the unselected cells of the memory at least twice in between the writing of the test content to the selected group of cells and the reading of the selected group of cells. **[FSM, state 36, Q and q]**

19. The device according to Claim 18, wherein the measurement circuit further operates, for at least one selected group of cells, to backup **[state 42]** the content of the selected group of cells and restore **[state 40]** the content of the selected group of cells with the backed up content following metering of the number of content errors.

20. The device according to Claim 18, further comprising:

a first and a second buffer memory connected to the dynamic random access memory; **CHO, CH1]**

wherein the write circuit writes the test content into the first buffer memory before writing to the selected group of cells **[state 32]**, and wherein the read circuit writes the read

content of the selected group of cells into the second buffer memory followed by reading the second buffer memory. **[state 38]**

21. The device according to Claim 19, wherein the measurement circuit performs the backup **[state 42]** in a predetermined part of the memory or else in an external backup memory. **[PM]**

22. The device according to Claim 20, wherein each selected group of cells forms a single page of the memory, **[see paragraph 54, CL RW]** and backing is made to one of the first and second buffer memories. **CH0 and CH1]**

23. The device according to Claim 18, wherein the memory refreshing circuit comprises:

a comparison circuit to compare the metered number of accumulated errors with a low threshold and a high threshold; **[CMP2]** and

a regulating circuit that increases the refresh period if the metered number of errors is less than the low threshold, decreases the refresh period if the metered number of errors is greater than the high threshold, and leaves the refresh period unchanged if the metered number of errors is greater than or equal to the low threshold and less than or equal to the high threshold. **[MRG, MUX2, +, -]**

24. The device according to Claim 18, wherein the memory refreshing circuit comprises:

a comparison circuit to compare the metered number of accumulated errors with a threshold; **[CMP2]** and

a regulating circuit to increase the refresh period if the metered number of errors is less than the threshold and decrease the refresh period if the metered number of errors is greater than or equal to the threshold. **[MRG, MUX2, +, -]**

25. The device according to Claim 24, further comprising storage means for storing a minimum limit value and a maximum limit value for the refresh period. **[SH2, SB2]**

26. The device according to Claim 15, wherein the memory refreshing circuit cyclically performs the measurement of the retention time of all the cells of the memory, and tags the cells of the memory having a lower retention as measured in the course of a measurement cycle, **[step 45]** and regulates the refresh period of the memory by setting the refresh period in the course of a next measurement cycle of the tagged cells to be refreshed more often than non-tagged cells of the memory. **[step 46]**

27. The device according to claim 15, wherein the device is incorporated into an apparatus **[TP]** which operates in both a standby mode and an active mode of operation, and wherein the memory refreshing circuit operates to measure and regulate during at least the course of the standby mode.

28. The device according to Claim 27, wherein the apparatus comprises a handset **[TP]** of a wireless communication system.

29. The device according to Claim 28, wherein the handset is a cellular mobile telephone. **[TP]**

30. A process for dynamically adjusting the refresh rate of a dynamic random access memory array, comprising:

selecting a group of memory cells within the memory, the selected group of memory cells comprising a sub-set of the entire memory array; **[states 30 and 41]**

measuring a test data content retention time for the selected group of memory cells at a measurement rate which exceeds a current refresh rate of the dynamic random access memory array; **[states 33-35 and 37-39]**

in the meantime, continuing to refresh the non-selected memory cells within the memory at the current refresh rate; **[state 36]** and

adjusting the current refresh rate based on the measured test data content retention time. **[Tref, MUX2 +,-]**

31. The process according to Claim 30, further comprising repeating the steps of claim 30 and selecting a different group of memory cells with each repeat so as to scan all of the cells of the memory. **[states 30 and 41]**

32 The process according to Claim 31, wherein adjusting comprises making an adjustment to the current refresh rate based on the measured test data content retention times for all groups of memory cells. **[MUX2]**

33. The process according to Claim 30, wherein the measurement rate is selected in comparison to the current refresh rate so as to refresh the non-selected memory cells at least twice before a test data content retention time measurement is made. **[state 36, Q and q]**

34. The process according to Claim 30, wherein measuring comprises:

writing test data to the selected group of memory cells; **[state 33]**

reading the test data from the selected group of memory cells after expiration of a delay set by the measurement rate; **[state 39]**

counting a number of content errors in the read test data. **[state 39]**

35. The process according to Claim 34, wherein adjusting comprises:

comparing the number of content errors to a threshold; **[RG2, NBE, >, <, CMP2]**

increasing the current refresh rate if the number is less than the threshold; **[CH, +, MUX2, RGT2]** and

decreasing the current refresh rate if the number more than the threshold. **[CB, -, MUX2, RGT2]**

36. The process according to Claim 34, further comprising repeating the steps of claim 30 and selecting a different group of memory cells with each repeat so as to scan all of the cells of the memory, and wherein counting comprises accumulating the number of content errors with each repeat. **[states 30 and 41, RG2, NBE, +, ACC]**

37. The process according to Claim 36, wherein adjusting comprises:
comparing the accumulated number of content errors to a threshold; **[CMP2]**
increasing the current refresh rate if the accumulated number is less than the threshold; **[Tref, +, MUX2]** and
decreasing the current refresh rate if the accumulated number more than the threshold. **[Tref, -, MUX2]**

38. A process for selectively adjusting refresh rate of a dynamic random access memory array, comprising:
successively selecting groups of memory cells within the memory, each selected group of memory cells comprising a sub-set of the entire memory array; **[states 30 and 41]**
measuring a test data content retention time for each selected group of memory cells; **[states 33-35 and 37-39]**
in the meantime, continuing to refresh the non-selected memory cells in accordance with their refresh rate; **[state 36]**
tagging certain ones of the selected groups of cells having a lower test data retention time; **[step 45]** and
adjusting the refresh rate for the memory cells such that tagged selected groups of memory cells are refreshed more frequently than non-tagged selected groups of memory cells. **[step 46]**

39. The process according to Claim 38, wherein measuring comprises:
writing test data to the selected group of memory cells; **[state 33]**
reading the test data from the selected group of memory cells after expiration of a delay; **[state 39]**
counting a number of content errors in the read test data. **[state 39]**

40. The process according to Claim 39, wherein tagging identifies certain ones of the selected groups of cells whose number of content errors exceeds a threshold. **[SH1, >, CMP2]**

41. The process according to Claim 38, further comprising regulating the refresh rate for non-tagged selected groups of memory cells based on the measured test data content retention times for all selected group of cells. **[Tref, MUX2, +,-]**

42. The process according to Claim 41, wherein regulating comprises:
writing test data to each selected group of memory cells; **[state 33]**
reading the test data from each selected group of memory cells after expiration of a delay;

[state 39]

accumulating a number of content errors in the read test data; **[ACC, RG2, state 39]**

comparing the accumulated number of content errors to a threshold; **[CMP2]**

increasing the refresh rate for non-tagged selected groups of memory cells if the accumulated number is less than the threshold; **[MUX2, +, SB1, <]** and

decreasing the refresh rate for non-tagged selected groups of memory cells if the accumulated number more than the threshold. **[MUX2, -, SH1, >]**